



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/996,510	11/27/2001	Kenneth Y. Chiu	5181-95300	2233

7590 02/10/2006

Rory D. Rankin
Conley, Rose & Tayon, P.C.
P.O. Box 398
Austin, TX 78767

EXAMINER

BRADLEY, MATTHEW A

ART UNIT	PAPER NUMBER
----------	--------------

2187

DATE MAILED: 02/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/996,510	Applicant(s) CHIU, KENNETH Y.	
	Examiner Matthew Bradley	Art Unit 2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 18 November 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-26 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-23 is/are rejected.
- 7) ☒ Claim(s) 24-26 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Amendment

This Office Action has been issued in response to amendment filed 18 November 2005.

Applicant's arguments have been carefully and fully considered in light of the instant amendment, but are not persuasive. Accordingly, this action has been made FINAL.

Claim Status

Original claims 1-23 and new claims 24-26 remain pending and are ready for examination.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-23 are rejected under 35 U.S.C. 102(e) as being anticipated by Khanna (U.S. 6,539,455) herein after referred to as Khanna.

As per independent claim 1, Khanna teach,

- receiving a transfer request which corresponds to a block of data, wherein
said block comprises a plurality of sub-blocks, said transfer request

comprising an address and a mask which indicates which of said sub-blocks are required as part of the request; (Column 22 lines 37-43). *The Examiner notes that Khanna teach of "loading" the CAM devices. The "loading" is acted upon by a "compare instruction" which the Examiner notes is a request that will produce a result that can then be transferred to the system issuing the "compare instruction." Accordingly, the "compare instruction", as taught by Khanna, is the transfer request as disclosed in the instant limitation.*

- generating a different address for each of said sub-blocks in response to receiving the transfer request; detecting which of said sub-blocks are required as part of said transfer request; and utilizing only those generated addresses which correspond to the sub-blocks which are required. (Column 22 line 66 to Column 23 line 5). *The Examiner notes that the system of Khanna completes the "compare instruction" as discussed supra, and with respect to the instant limitations, the system then proceeds to "output the match index of the location in its CAM array." The "location" will contain an address in memory that corresponds to the matched entry of the "compare instruction". Accordingly, each individual entry, will have an address generated that corresponds to its individual location in memory.*

As per dependent claim 2, Khanna teach, "wherein detecting which of said sub-blocks are required comprises examining said mask" (Column 17 lines 45-55). *The*

Examiner notes that Khanna teach of "prefix mask data" that is relied upon to indicate whether the data in a specific memory cell should be masked. Accordingly, the mask as disclosed in the instant claim is contained within the "prefix mask data" as taught by Khanna.

As per dependent claim 3, Khanna teach, "wherein said mask comprises a separate bit for each of said sub-blocks, wherein a bit with a first value indicates a corresponding sub-block is required, and wherein a bit with a second value indicates a corresponding sub-block is not required" (Column 17 lines 45-55). *As discussed supra, with respect to the "prefix mask data", a determination is made as to whether or not the system will rely on the data in a specific memory cell. Accordingly, the Examiner further notes that the "prefix mask data" must include a bit, or logic 'high' or 'low', that communicates to the system whether the sub-block is required or not.*

As per dependent claim 4, Khanna teach, "wherein said request includes an address corresponding to said block, and wherein said transfer comprises transferring one of said sub-blocks at a time" (Column 22 lines 37-43).

As per dependent claim 5, Khanna teach, "wherein each of said addresses corresponding to said sub-blocks are generated concurrently" (Column 22 lines 37-43). *The Examiner notes that as discussed supra, addresses will be generated based upon the "compare instruction". If there are two matches, then the addresses will be generated at the same time based upon the instruction. Accordingly, the addresses will be 'generated concurrently.'*

As per dependent claim 6, Khanna teach, "wherein said detecting comprises: detecting a first bit of said mask which has a first value, wherein said first bit corresponds to a first sub-block; and selecting a first address of said generated addresses which corresponds to the first sub-block" (Column 17 lines 45-55).

As per dependent claim 7, Khanna teach, "wherein said detecting further comprises: masking off said first bit of said mask, subsequent to utilizing said first address; detecting a second bit of said mask which has a first value, wherein said second bit corresponds to a second sub-block; and selecting a second address of said generated addresses which corresponds to the second sub-block" (Column 17 lines 45-55).

As per dependent claim 8, Khanna teach, "determining a first number of said sub-blocks are required; and detecting transfer of all said required sub-blocks are complete, in response to detecting a number of sub-blocks equal to said first number have been transferred" (Column 22 line 66 to Column 23 line 5). *The Examiner notes that as discussed supra, matches from the "compare instruction" will be generated and passed on. In order for the system to maintain accurate results, an equal number of matches that are detected must be passed on (transferred) back to the system of Khanna to further select the best match.*

As per independent claim 9, the Examiner notes that in addition to the limitations as discussed supra with respect to independent claim 1, the instant claim further recites a first interface and a second interface embodied on a device. Khana et al teaches a

first interface as “mask cells” (see column 5 lines 9-10) and a second interface as a “CAM match line” (see column 5 lines 8-12).

As per dependent claim **10**, Khanna teach, “wherein said second interface is further configured to detect which of said sub-blocks are required by examining said mask” (Column 17 lines 45-55). *The Examiner notes that Khanna teach of “prefix mask data” that is relied upon to indicate whether the data in a specific memory cell should be masked. Accordingly, the mask as disclosed in the instant claim is contained within the “prefix mask data” as taught by Khanna.*

As per dependent claim **11**, Khanna teach, “wherein said mask comprises a separate bit for each of said sub-blocks, wherein a bit with a first value indicates said corresponding sub-block is required, and wherein a bit with a second value indicates said corresponding sub-block is not required” (Column 17 lines 45-55). *As discussed supra, with respect to the “prefix mask data”, a determination is made as to whether or not the system will rely on the data in a specific memory cell. Accordingly, the Examiner further notes that the “prefix mask data” must include a bit, or logic ‘high’ or ‘low’, that communicates to the system whether the sub-block is required or not.*

As per dependent claim **12**, Khanna teach, “wherein said request includes an address corresponding to said block, and wherein said second interface is configured to initiate transfer of only one of said sub-blocks at a time” (Column 22 lines 37-43).

As per dependent claim **13**, Khanna teach, “wherein said second interface is configured to generate each of said addresses corresponding to said sub-blocks concurrently” (Column 22 lines 37-43). *The Examiner notes that as discussed supra,*

addresses will be generated based upon the "compare instruction". If there are two matches, then the addresses will be generated at the same time based upon the instruction. Accordingly, the addresses will be 'generated concurrently.'

As per dependent claim **14**, Khanna teach, "wherein said second interface is configured to detect which of said sub-blocks are required by: detecting a first bit of said mask which has a first value, wherein said first bit corresponds to a first sub-block; and selecting a first address of said generated addresses which corresponds to the first sub-block" (Column 17 lines 45-55).

As per dependent claim **15**, Khanna teach, "wherein said second interface is further configured to detect said required sub-blocks by: masking off said first bit of said mask, subsequent to utilizing said first address; detecting a second bit of said mask which has a first value, wherein said second bit corresponds to a second sub-block; and selecting a second address of said generated addresses which corresponds to the second sub-block" (Column 17 lines 45-55).

As per dependent claim **16**, Khanna teach, "wherein said second interface is further configured to: determine a first number of said sub-blocks are required; and detect transfer of all said required sub-blocks are complete, in response to detecting a number of sub-blocks equal to said first number have been transferred" (Column 22 line 66 to Column 23 line 5). *The Examiner notes that as discussed supra, matches from the "compare instruction" will be generated and passed on. In order for the system to maintain accurate results, an equal number of matches that are detected must be passed on (transferred) back to the system of Khanna to further select the best match.*

As per independent claim **17**, Khanna teach,

- a control unit, wherein said control unit is configured to control access to a plurality of blocks of data, wherein each of said blocks of data comprise a plurality of sub-blocks, and wherein said control unit is not configured to convey a full block of said blocks of data at one time; (Column 5 lines 9-10) *The Examiner notes that the CAM cells are connected via a bus as shown in Figure 8A items 806 and 812. The Examiner further notes that in all computing systems, the memory cells are connected to a controller or processor. Accordingly, the 'control unit' as found in the instant claim is the controller or processor to which the memory cells are connected to via said bus.*
- a first interface coupled to said control unit, wherein said interface is configured to: (Column 5 lines 9-10)
- receive a transfer request, wherein said request corresponds to a first block of said blocks of data, said transfer request comprising an address and a mask which indicates which of said sub-blocks are required as part of the request; (Column 22 lines 37-43). *The Examiner notes that Khanna teach of "loading" the CAM devices. The "loading" is acted upon by a "compare instruction" which the Examiner notes is a request that will produce a result that can then be transferred to the system issuing the "compare instruction." Accordingly, the "compare instruction", as taught by Khanna, is the transfer request as disclosed in the instant limitation.*

- generate a different address corresponding to each sub-block of said first block in response to receiving the transfer request; detect which of said sub-blocks are required as part of said transfer request; and utilize only those generated addresses which correspond to the sub-blocks which are required. (Column 22 line 66 to Column 23 line 5). *The Examiner notes that the system of Khanna completes the "compare instruction" as discussed supra, and with respect to the instant limitations, the system then proceeds to "output the match index of the location in its CAM array." The "location" will contain an address in memory that corresponds to the matched entry of the "compare instruction". Accordingly, each individual entry, will have an address generated that corresponds to its individual location in memory.*

As per dependent claim **18**, Khanna teach, "detect which of said sub-blocks are required by examining said mask" (Column 17 lines 45-55). *The Examiner notes that Khanna teach of "prefix mask data" that is relied upon to indicate whether the data in a specific memory cell should be masked. Accordingly, the mask as disclosed in the instant claim is contained within the "prefix mask data" as taught by Khanna.*

As per dependent claim **19**, Khanna teach, "wherein said mask comprises a plurality of bits, each of which correspond to a different sub-block of said first block, wherein a bit with a first value indicates said corresponding sub-block is required, and wherein a bit with a second value indicates said corresponding sub-block is not required" (Column 17 lines 45-55). *As discussed supra, with respect to the "prefix mask*

data”, a determination is made as to whether or not the system will rely on the data in a specific memory cell. Accordingly, the Examiner further notes that the “prefix mask data” must include a bit, or logic ‘high’ or ‘low’, that communicates to the system whether the sub-block is required or not.

As per dependent claim **20**, Khanna teach, “wherein said first interface is configured to generate each of said addresses corresponding to said sub-blocks concurrently” (Column 22 lines 37-43). *The Examiner notes that as discussed supra, addresses will be generated based upon the “compare instruction”. If there are two matches, then the addresses will be generated at the same time based upon the instruction. Accordingly, the addresses will be ‘generated concurrently.’*

As per dependent claim **21**, Khanna teach, “wherein said first interface is configured to detect which of said sub-blocks are required by: detecting a first bit of said mask which has a first value, wherein said first bit corresponds to a first sub-block; and selecting a first address of said generated addresses which corresponds to the first sub-block” (Column 17 lines 45-55).

As per dependent claim **22**, Khanna teach, “wherein said first interface is further configured to: mask off said first bit of said mask, subsequent to utilizing said first address; detect a second bit of said mask which has a first value, wherein said second bit corresponds to a second sub-block; and select a second address of said generated addresses which corresponds to the second sub-block” (Column 17 lines 45-55).

As per dependent claim **23**, Khanna teach, “wherein said first interface is further configured to: determine a first number of said sub-blocks are required; and detect

transfer of all said required sub-blocks are complete, in response to detecting a number of sub-blocks equal to said first number have been transferred" (Column 22 line 66 to Column 23 line 5). *The Examiner notes that as discussed supra, matches from the "compare instruction" will be generated and passed on. In order for the system to maintain accurate results, an equal number of matches that are detected must be passed on (transferred) back to the system of Khanna to further select the best match.*

Allowable Subject Matter

Claim **24** is objected to as being dependent upon rejected base claim **1**, claim **25** is objected to as being dependent upon rejected base claim **9**, claim **26** is objected to as being dependent upon rejected base claim **17**, but would be allowable if rewritten in correct and independent form including all of the limitations of the respective base claims and any intervening claims.

The following is an Examiner's statement of reasons for allowance: the prior art teaches the block selection as claimed, but fails to teach the combination including the limitation of:

(Claim **24**) "...wherein a number of sub-blocks required as part of the transfer request is equal to a sum of the number of bits which are asserted in the mask."

(Claim **25**) "...wherein a number of sub-blocks required as part of the transfer request is equal to a sum of the number of bits which are asserted in the mask."

(Claim **26**) "...wherein a number of sub-blocks required as part of the transfer request is equal to a sum of the number of bits which are asserted in the mask."

If the applicant should choose to rewrite the independent claims to include the limitations recited in the dependent claims, the applicant is then encouraged to amend the title of the invention such that it is descriptive of the invention as claimed, as required by sec. 606.01 of the MPEP. Furthermore, the summary of the invention and the abstract should be amended to bring them into harmony with the allowed claims as required by paragraph 2 of sec. 1302.01 of the MPEP.

As allowable subject matter has been indicated, applicant's response must either comply with all formal requirements or specifically traverse each requirement not complied with. See 37 C.F.R. § 1.111(b) and § 707.07(a) of the MPEP.

Response to Arguments

Applicant's arguments filed 18 November 2005 have been carefully and fully considered, but are not persuasive. As such this action has been made FINAL.

With respect to the applicant's arguments located within the last paragraph on page 9 of the instant remarks which recites:

'In contrast, Khanna does not disclose a transfer request which includes an address and a mask.'

The Examiner respectfully disagrees. As taught by Khanna, each CAM of Khanna is loaded with addresses and prefix mask data. When the compare instruction is issued to the CAM, the addresses issued in the instruction are compared with the addresses stored in the CAM. Before this is done, the addresses and prefix mask data are loaded and then the comparison takes place. Utilizing the mask, the addresses are selected, which compare successfully. Therefore, the compare instruction requires the use of the prefix mask data and addresses previously stored in order for the compare

instruction to even take place. The loading of the addresses and prefix mask data are part of the compare instruction as they are done BEFORE the compare instruction is executed.

With respect to applicant's arguments drawn to claim 9 and 17, the Examiner incorporates by reference herein the remarks made supra with respect to claim 1.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew Bradley whose telephone number is (571) 272-8575. The examiner can normally be reached on 6:30-3:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald A. Sparks can be reached on (571) 272-4201. The fax phone

Art Unit: 2187

number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DAS/mb



DONALD SPARKS
SUPERVISORY PATENT EXAMINER